

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claim 1, and add new claims 58-84, as follows:

Listing of Claims:

1-57. (Cancelled)

58. (New) A method of refreshing dynamic data stored in an integrated circuit, the integrated circuit adapted to operate in a self-refresh mode of operation to refresh the dynamic data at a refresh time that defines how often the dynamic data is refreshed during the self-refresh mode, the method comprising:

monitoring a magnitude of a voltage applied to the integrated circuit; and

during the self-refresh mode of operation, increasing a frequency of a self-refresh clock signal as the magnitude of the voltage applied to the integrated circuit decreases to decrease the refresh time, the self-refresh clock signal defining the refresh time.

59. (New) The method of claim 58 wherein monitoring the magnitude of the voltage applied to the integrated circuit comprises detecting whether the magnitude is less than or equal to a minimum voltage level.

60. (New) The method of claim 59 wherein increasing the frequency of the self-refresh clock signal as a function of the magnitude of the voltage applied to the integrated circuit comprises increasing the frequency of the self-refresh clock signal in response to the magnitude of the voltage applied to the integrated circuit being less than or equal to the minimum voltage level.

61. (New) The method of claim 58 wherein monitoring the magnitude of the supply voltage comprises detecting whether the magnitude of the voltage applied to the

integrated circuit is less than or equal to a minimum supply voltage, and increasing the frequency of the self-refresh clock as a function of the magnitude of the voltage applied to the integrated circuit comprises increasing the frequency of the self-refresh clock as a function of decreases in the magnitude of the voltage applied to the integrated circuit once the detected magnitude is less than or equal to the minimum supply voltage.

62. (New) The method of claim 61 wherein increasing the frequency of the self-refresh clock signal as a function decreases in the magnitude of the voltage applied to the integrated circuit once the detected magnitude is less than or equal to the minimum supply voltage comprises generating a bias voltage from the voltage applied to the integrated circuit, the bias voltage having a value that is inversely related to the refresh time, and increasing the bias voltage as a function of decreases in the voltage applied to the integrated circuit once the detected magnitude is less than or equal to the minimum supply voltage.

63. (New) The method of claim 58 wherein the voltage applied to the integrated circuit comprises a supply voltage applied to the integrated circuit.

64. (New) The method of claim 58 wherein increasing the frequency of the self-refresh clock signal as the magnitude of the voltage applied to the integrated circuit decreases comprises linearly increasing the frequency of the self-refresh clock signal as a function of the magnitude of the voltage applied to the integrated circuit.

65. (New) A method for controlling a refresh rate of dynamic data, the method comprising:

receiving an input voltage having a magnitude that is indicative of a mode of operation, the mode of operation including a normal mode and a low-power mode;

in the normal mode, generating a refresh bias voltage having a substantially constant value;

in the low-power mode, adjusting the value of the refresh bias voltage as a function of the magnitude of the input voltage;

developing a refresh clock signal having a frequency that is a function of the refresh bias voltage; and

in response to the refresh clock signal, developing refresh signals that control the refresh rate of the dynamic data as a function of the frequency of the refresh clock signal.

66. (New) The method of claim 65 wherein the magnitude of the input voltage being greater than a minimum value is indicative of the normal mode of operation and the magnitude of the input voltage being less than or equal to the minimum value is indicative of the low-power mode of operation.

67. (New) The method of claim 65 wherein adjusting the value of the refresh bias voltage comprises adjusting the bias voltage as a linear function of the magnitude of the input voltage.

68. (New) The method of claim 65 wherein developing the refresh clock signal having a frequency that is a function of the refresh bias comprises increasing the frequency of the refresh clock signal as the bias voltage decreases and decreasing the frequency of the refresh clock signal as the bias voltage increases.

69. (New) The method of claim 65, further comprising generating row and bank addresses responsive to the refresh clock signal and at a rate that is a function of the frequency of the refresh clock signal and the refresh rate being a function of the rate at which the row and bank addresses are generated.

70. (New) A method for controlling a refresh rate of dynamic data, the method comprising:

receiving an input voltage having a magnitude that is indicative of a mode of operation, the mode of operation including a normal mode and a low-power mode;

in the normal mode, generating a refresh bias voltage having a substantially constant value;

in the low-power mode, outputting the input voltage as the bias voltage;

developing a refresh clock signal having a frequency that is a function of the refresh bias voltage; and

in response to the refresh clock signal, developing refresh signals that control the refresh rate of the dynamic data as a function of the frequency of the refresh clock signal.

71. (New) The method of claim 70 wherein the magnitude of the input voltage being greater than a minimum value is indicative of the normal mode of operation and the magnitude of the input voltage being less than or equal to the minimum value is indicative of the low-power mode of operation.

72. (New) The method of claim 70 wherein developing the refresh clock signal having a frequency that is a function of the refresh bias comprises increasing the frequency of the refresh clock signal as the bias voltage increases and decreasing the frequency of the refresh clock signal as the bias voltage decreases.

73. (New) The method of claim 70, further comprising generating row and bank addresses responsive to the refresh clock signal and at a rate that is a function of the frequency of the refresh clock signal and the refresh rate being a function of the rate at which the row and bank addresses are generated.

74. (New) A method for controlling a refresh rate of dynamic data in an integrated circuit, the method comprising:

receiving an input voltage having a magnitude that is indicative of a mode of operation, the mode of operation including a normal mode and a low-power mode;

in the normal mode, generating a refresh bias voltage having a substantially constant value;

in the low-power mode, adjusting the value of the refresh bias voltage as a function of the magnitude of the input voltage in response to a bias adjustment command that is generated external to the integrated circuit;

developing a refresh clock signal having a frequency that is a function of the refresh bias voltage; and

in response to the refresh clock signal, developing refresh signals that control the refresh rate of the dynamic data as a function of the frequency of the refresh clock signal.

75. (New) The method of claim 74, further comprising generating a load mode register command for the bias voltage adjustment command.

76. (New) The method of claim 74 wherein the magnitude of the input voltage being greater than a minimum value is indicative of the normal mode of operation and the magnitude of the input voltage being less than or equal to the minimum value is indicative of the low-power mode of operation.

77. (New) The method of claim 74 wherein adjusting the value of the refresh bias voltage comprises adjusting the bias voltage as a linear function of the magnitude of the input voltage.

78. (New) The method of claim 74 wherein developing the refresh clock signal having a frequency that is a function of the refresh bias comprises increasing the

frequency of the refresh clock signal as the bias voltage decreases and decreasing the frequency of the refresh clock signal as the bias voltage increases.

79. (New) The method of claim 74, further comprising generating row and bank addresses responsive to the refresh clock signal and at a rate that is a function of the frequency of the refresh clock signal and the refresh rate being a function of the rate at which the row and bank addresses are generated.

80. (New) A method for controlling a refresh rate of dynamic data, the method comprising:

receiving an input voltage having a magnitude that is indicative of a mode of operation, the mode of operation including a normal mode, a first low-power mode, and a second low-power mode;

in the normal mode, generating a refresh bias voltage having a substantially constant value;

in the first low-power mode, adjusting the value of the refresh bias voltage as a function of the magnitude of the input voltage;

in the second low-power mode, outputting the input voltage as the bias voltage;

developing a refresh clock signal having a frequency that is a function of the refresh bias voltage; and

in response to the refresh clock signal, developing refresh signals that control the refresh rate of the dynamic data as a function of the frequency of the refresh clock signal.

81. (New) The method of claim 80 wherein the magnitude of the input voltage being greater than a first minimum value is indicative of the normal mode of operation, the magnitude of the input voltage being less than or equal to the first minimum value and greater than a second minimum value is indicative of the first low-power mode of operation, and the magnitude of the input voltage being less than or equal to the second minimum value is indicative of the second low-power mode of operation.

82. (New) The method of claim 81 wherein adjusting the value of the refresh bias voltage comprises adjusting the bias voltage as a linear function of the magnitude of the input voltage.

83. (New) The method of claim 81 wherein developing the refresh clock signal having a frequency that is a function of the refresh bias comprises increasing the frequency of the refresh clock signal as the bias voltage increases and decreasing the frequency of the refresh clock signal as the bias voltage decreases.

84. (New) The method of claim 81, further comprising generating row and bank addresses responsive to the refresh clock signal and at a rate that is a function of the frequency of the refresh clock signal and the refresh rate being a function of the rate at which the row and bank addresses are generated.